PATENT
Attorney Docket No. 401322/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KUROOKA et al.

Application No. Unknown

Filed: August 3, 2001

For: TRACE CIRCUIT

Art Unit: Unknown

Examiner: Unknown

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 4 with:

This invention relates to a trace circuit built into a debugging circuit which is, in turn, built into a microcomputer of a device.

Replace the paragraph beginning at page 1, line 20 with:

In a general microcomputer-embedded-typed LSI, the address bus and data bus and so on for connecting to the memory of the ICE are not connected to the LSI terminal. This is because the program is stored in a memory embedded in the microcomputer. Therefore, a mode only used for ICE connection is prepared. An address bus and a data bus are extended from the external terminal of the LSI. In addition, the original function, with the terminal used as an address bus and a data bus, is carried out within the ICE.

Replace the paragraph beginning at page 2, line 4 with:

However, because several terminals of the microcomputer need to be connected between the ICE and the target system, the connection between ICE and the target system has

become difficult, accompanying an improvement in speed of a microcomputer or a multi-bit bus. Furthermore, the various functions for system realization, other than a microcomputer, are embedded in LSI in a system LSI in which a microcomputer is embedded, so that it has become difficult to emulate the original function which the terminal used as an address bus or a data bus for connection with the memory of ICE has, using the ICE.

Replace the paragraph beginning at page 2, line 15 with:

The debugging circuit performing the function, which the ICE conventionally has on the basis of the foregoing description, is embedded in a microcomputer, and a program development technique has been adopted such that the emulator (debugger) is connected to a host computer through an LSI terminal only used for debugging.

Replace the paragraph beginning at page 2, line 21 with:

Fig. 6 shows an internal circuit arrangement of the conventional microcomputer-embedded LSI 1. Reference numeral 2 denotes a bus interface. Reference numeral 3 denotes a CPU. Reference numeral 4 denotes a memory. Reference numeral 5 denotes a debugging circuit. Reference numeral 6 denotes a trace circuit in the debugging circuit. Reference numeral 7 denotes a control circuit (event control circuit). Reference numeral 8 denotes a trace buffer memory. Reference numeral 9 denotes an output latching circuit. Reference numeral 10 denotes an output control circuit. Reference numeral 11 denotes a control bus. Reference numeral 12 denotes an address bus. Reference numeral 13 denotes a data bus. Reference numeral 14 denotes a control bus. Reference numeral 15 denotes an address bus. Reference numeral 16 denotes a data bus. Reference numerals 14, 15 and 16 denote trace buses. Data is output from the trace circuit 6 through the LSI data output terminal DATA. This data is constituted by 4 bits.

Replace the paragraph beginning at page 3, line 14 with:

Fig. 7 shows a timing chart of various signals in this trace circuit 6. Any desired data (8 bits) of the control bus 14, the address bus 15, and the data bus 16 is stored in the trace buffer memory 8 through the event control circuit 7 based on a signal WRITE that is synchronized with the bus clock signal CK. The data once D stored in the trace buffer memory 8 is output, based on subsequent READ signals, from the trace buffer memory 8 to the output latch circuit 9 and is further input into the output control circuit 10. The output control circuit 10 converts 8- bit data to 4-bit data, which is output through the terminal DATA, using the output control signals S1 and S2, each of whose frequency is the same as

the bus clock signal CK frequency and whose phase is shifted by only π through the terminal DATA. In Fig. 7, ABh, CDh, 12h, 34h are hexadecimal numbers. Furthermore, in Fig. 6 and Fig. 7, A1, A2, A3, and A4 are 8-bit data stored in sequence in the trace buffer memory 8.

Replace the paragraph beginning at page 4, line 6 with:

However, the processing speed of the microcomputer in the system LSI in recent years is becoming faster and the bus clock frequency therein is increasing. As a result, in the conventional case, access speed to a trace buffer memory cannot catch up with the speed at which data is transmitted from the control circuit. In other words, since one bus cycle is becoming shorter and shorter, it is becoming difficult to store the input data in the trace buffer memory or to output the data from it during one bus cycle.

Replace the paragraph beginning at page 5, line 15 with:

Fig. 2 shows time charts of various signals for explaining operation of the first embodiment.

Replace the paragraph beginning at page 5, line 17 with:

Fig. 3 shows time charts of various signals for explaining operation of the second embodiment of this invention.

Replace the paragraph beginning at page 5, line 22 with:

Fig. 5 shows time charts of various signals for explaining operation of the third embodiment.

Replace the paragraph beginning at page 6, line 1 with:

Fig. 7 shows time charts of various signals for explaining operation of the conventional circuit.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A trace circuit built into a debugging circuit that is, in turn, built into a microcomputer for program debugging, said trace circuit tracing data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator, said trace circuit comprising:

plural trace buffer memories in which the data on the bus of the microcomputer is stored according to the bus clock signal; and

a control circuit storing the data on the bus in said trace buffer memories, cyclically and in a predetermined order, outputting the data stored in said trace buffer memories, cyclically, and in a predetermined order, wherein the storage of data in and output of data from said trace buffer memories is synchronized with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to the emulator.

2. (Amended) The trace circuit according to claim 1, wherein said control circuit checks the number of bits of the data on said bus, and, if the number of bits of the data on said bus is no larger than a predetermined value, said control circuit stores the data on the bus in only some of said trace buffer memories, and outputs the data stored in said trace buffer memories, cyclically and in predetermined order.

4. (Amended) The trace circuit according to claim 1 further comprising a bit width conversion circuit connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on bit width of the emulator.

5. (Amended) The trace circuit according to claim 1 further comprising output latch circuits in a number equal to the number of said trace buffer memories and connected between respective trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch outputs of said trace buffer memories.

6. (Amended) A trace circuit built into a debugging circuit that is, in turn, built into a microcomputer for program debugging, said trace circuit tracing data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator, said trace circuit comprising:

two trace buffer memories in which the data on the bus of the microcomputer is stored according to the bus clock signal; and

a control circuit storing the data on the bus in said trace buffer memories cyclically and alternately, outputting the data stored from said trace buffer memories cyclically and alternately, wherein the storage of data in and output of data from said trace buffer memories is synchronized with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to the emulator.

7. (Amended) The trace circuit according to claim 6, wherein said control circuit checks the number of bits of the data on the bus, and, if the number of bits of the data on the bus is no larger than a predetermined value, said control circuit stores the data on the bus in only some of said trace buffer memories, and outputs the data stored in said trace buffer memories, cyclically and in predetermined order.

9. (Amended) The trace circuit according to claim 6 further comprising a bit width conversion circuit connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on bit width of the emulator.

10. (Amended) The trace circuit according to claim 6 further comprising two output latch circuits respectively connected between said two trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch outputs of said trace buffer memories.

IN THE ABSTRACT:

Replace the Abstract with:

ABSTRACT OF THE DISCLOSURE

A trace circuit includes the event control circuit and two trace buffer memories. The event control circuit receives data on a control bus, an address bus, and data a bus and stores the data cyclically and alternately in the two buffer memories. Also, the event control circuit makes the two buffer memories output the stored data cyclically and alternately.

REMARKS

The foregoing Amendment corrects translational errors and conforms the claims to United States practice.

Respectfully submitted,

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AMENDMENTS TO SPECIFICATION, CLAIMS AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 1, line 4:

This invention relates to a trace circuit ~~built-in~~ built into a debugging circuit which is, in turn, ~~built-in~~ built into a microcomputer of a device.

Amendments to the paragraph beginning at page 1, line 20:

In a general microcomputer-embedded-typed LSI, the address bus and data bus and so on for connecting to the memory of the ICE are not connected to the LSI terminal. This is because~~,~~ the program is stored in a memory embedded in the microcomputer. Therefore, a mode only used for ICE connection is prepared. An address bus and a data bus are extended from the external terminal of the LSI. In addition, the original function ~~which~~, with the terminal used as an address bus and a data bus ~~has~~, is carried out within the ICE.

Amendments to the paragraph beginning at page 2, line 4:

However, because several ~~numbers of~~ terminals of the microcomputer need to be connected between the ICE and the target system, the connection between ICE and the target system has become difficult, accompanying ~~with~~ an improvement ~~of high~~ in speed of a microcomputer or a multi-bit bus. Furthermore, the various functions for system realization, other than a microcomputer, are embedded in LSI in a system LSI in which a microcomputer is embedded, so that it has become difficult to emulate the original function which the terminal used as an address bus or a data bus for connection with the memory of ICE has, using the ICE.

Amendments to the paragraph beginning at page 2, line 15:

The debugging circuit performing the function, which the ICE conventionally has on the basis of the ~~above backgrounds~~ foregoing description, is embedded in a microcomputer, and a program development technique has been adopted such that the emulator (debugger) is connected to a host computer through ~~the~~ an LSI terminal only used for debugging.

Amendments to the paragraph beginning at page 2, line 21:

Fig. 6 shows an internal circuit arrangement of the conventional microcomputer-embedded ~~-typed~~ LSI 1. Reference numeral 2 denotes a bus interface. Reference numeral 3 denotes a CPU. Reference numeral 4 denotes a memory. Reference numeral 5 denotes a debugging circuit. Reference numeral 6 denotes a trace circuit in the debugging circuit. Reference numeral 7 denotes a control circuit (event control circuit). Reference numeral 8 denotes a trace buffer memory. Reference numeral 9 denotes an output latching circuit. Reference numeral 10 denotes an output control circuit. Reference numeral 11 denotes a control bus. Reference numeral 12 denotes an address bus. Reference numeral 13 denotes a data bus. Reference numeral 14 denotes a control bus. Reference numeral 15 denotes an address bus. Reference numeral 16 denotes a data bus. Reference numerals 14, 15 and 16 denote trace buses. Data is output from the trace circuit 6 through the LSI data output terminal DATA. This data is constituted by 4 bits.

Amendments to the paragraph beginning at page 3, line 14:

Fig. 7 shows a timing chart of various signals in this trace circuit 6. Any desired data (8 bits) of the control bus 14, the address bus 15, and the data bus 16 is stored in the trace buffer memory 8 through the event control circuit 7 based on a signal WRITE that is synchronized with the bus clock signal CK. The data once D stored in the trace buffer memory 8 is output, based on subsequent READ signals, from the trace buffer memory 8 to the output latch circuit 9 and is further input into the output control circuit 10. The output control circuit 10 converts 8- bit data to 4-bit data, which is output through the terminal DATA, using the output control signals S1 and S2, each of whose frequency is ~~as~~ the same as the bus clock signal CK frequency and whose phase is shifted by only π through the terminal DATA. In Fig. 7, ABh, CDh, 12h, 34h are hexadecimal numbers. Furthermore, in Fig. 6 and Fig. 7, A1, A2, A3, and A4 are 8-bit data stored in sequence in the trace buffer memory 8.

Amendments to the paragraph beginning at page 4, line 6:

However, the processing speed of the microcomputer in the system LSI in recent years is becoming faster and the bus clock frequency therein is increasing. As a result, in the conventional case, access speed to a trace buffer memory cannot catch up with the speed at which data is transmitted from the control circuit. In other words, since one bus cycle is becoming shorter and shorter, it is becoming difficult to store the input data in the trace buffer memory or to output the data from it during ~~the~~ one bus cycle.

Amendments to the paragraph beginning at page 5, line 15:

Fig. 2 shows ~~the~~ time charts of ~~the~~ various signals for explaining operation ~~in~~ of the first embodiment.

Amendments to the paragraph beginning at page 5, line 17:

Fig. 3 shows ~~the~~ time charts of ~~the~~ various signals for explaining operation ~~in~~ of the second embodiment of this invention.

Amendments to the paragraph beginning at page 5, line 22:

Fig. 5 shows ~~the~~ time charts of ~~the~~ various signals for explaining operation ~~in~~ of the third embodiment.

Amendments to the paragraph beginning at page 6, line 1:

Fig. 7 shows ~~the~~ time charts of ~~the~~ various signals for explaining operation ~~in~~ of the conventional circuit.

Amendments to existing claims:

1. (Amended) A trace circuit ~~built in~~ built into a debugging circuit that is, in turn, ~~built in~~ built into a microcomputer ~~and performs~~ for program debugging, said trace circuit tracing data on a bus of ~~said~~ the microcomputer according to a bus clock signal and outputting ~~the~~a result to an emulator, said trace circuit comprising:

plural trace buffer memories in which the data on ~~said~~ the bus of ~~said~~ the microcomputer is stored according to the bus clock signal; and

a control circuit ~~which makes~~ storing the data on the bus in said trace buffer memories ~~store~~, cyclically and in a predetermined order ~~the data on said bus, makes~~ outputting the data stored in said trace buffer memories ~~output~~, cyclically, and in a predetermined order ~~the stored data~~, wherein the storage of data in and output of data from said trace buffer memories is ~~performed in synchronization~~ synchronized with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to ~~said~~ the emulator.

2. (Amended) The trace circuit according to claim 1, wherein said control circuit checks the number of bits of the data on said bus, and, if the number of bits of the data on said bus is ~~equal to or smaller~~ no larger than a predetermined value, said control circuit ~~makes~~stores the data on the bus in only some of said trace buffer memories ~~stores the data on said bus~~, and ~~makes~~ outputs the data stored in said trace buffer memories, ~~in which the data is stored, output the data~~ cyclically and in predetermined order.

4. (Amended) The trace circuit according to claim 1 further comprising a bit width conversion circuit ~~provided~~ connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on ~~the~~ bit width ~~acceptable to said~~ of the emulator.

5. (Amended) The trace circuit according to claim 1 further comprising output latch circuits in a number equal to the number of said trace buffer memories and ~~provided~~ connected between respective ~~said~~ trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch ~~the output~~ outputs of said trace buffer memories.

6. (Amended) A trace circuit ~~built in~~ built into a debugging circuit that is, in turn, ~~built in~~ built into a microcomputer ~~and performs~~ for program debugging, said trace circuit tracing data on a bus of ~~said~~ the microcomputer according to a bus clock signal and outputting ~~thea~~ result to an emulator, said trace circuit comprising:

two trace buffer memories in which the data on ~~said~~ the bus of ~~said~~ the microcomputer is stored according to the bus clock signal; and

a control circuit ~~which makes~~ storing the data on the bus in said trace buffer memories ~~store~~ cyclically and alternately ~~the data on said bus, makes~~ outputting the data stored from said trace buffer memories ~~output~~ cyclically and alternately ~~the stored data~~, wherein the storage of data in and output of data from said trace buffer memories is ~~performed in synchronization~~synchronized with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to ~~said~~ the emulator.

7. (Amended) The trace circuit according to claim 6, wherein said control circuit checks the number of bits of the data on ~~said~~ the bus, and, if the number of bits of the data on ~~said~~ the bus is ~~equal to or smaller~~ no larger than a predetermined value, said control circuit ~~makes~~stores the data on the bus in only some of said trace buffer memories ~~stores the data on said bus~~, and ~~makes~~ outputs the data stored in said trace buffer memories, ~~in which the data is stored, output the data~~ cyclically and in predetermined order.

9. (Amended) The trace circuit according to claim 6 further comprising a bit width conversion circuit ~~provided~~ connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on ~~the~~ bit width ~~acceptable to said~~ of the emulator.

10. (Amended) The trace circuit according to claim 6 further comprising two output latch circuits ~~provided~~ respectively connected between ~~respective~~ said two trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch ~~the output~~ outputs of said trace buffer memories.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

~~The~~A trace circuit ~~comprises~~ includes the event control circuit and ~~tow~~ two trace buffer memories. The event control circuit receives data on ~~the~~ a control bus, an address bus, and data a bus and ~~makes~~ stores the data ~~stored~~ cyclically and alternately in the two buffer memories. Also, the event control circuit makes the two buffer memories output the ~~store~~ stored data cyclically and alternately.

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PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A trace circuit built into a debugging circuit that is, in turn, built into a microcomputer for program debugging, said trace circuit tracing data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator, said trace circuit comprising:

plural trace buffer memories in which the data on the bus of the microcomputer is stored according to the bus clock signal; and

a control circuit storing the data on the bus in said trace buffer memories, cyclically and in a predetermined order, outputting the data stored in said trace buffer memories, cyclically, and in a predetermined order, wherein the storage of data in and output of data from said trace buffer memories is synchronized with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to the emulator.

2. The trace circuit according to claim 1, wherein said control circuit checks the number of bits of the data on said bus, and, if the number of bits of the data on said bus is no larger than a predetermined value, said control circuit stores the data on the bus in only some of said trace buffer memories, and outputs the data stored in said trace buffer memories, cyclically and in predetermined order.

3. The trace circuit according to claim 2, wherein the predetermined value is 4 bits.

4. The trace circuit according to claim 1 further comprising a bit width conversion circuit connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on bit width of the emulator.

5. The trace circuit according to claim 1 further comprising output latch circuits in a number equal to the number of said trace buffer memories and connected between respective trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch outputs of said trace buffer memories.

6. A trace circuit built into a debugging circuit that is, in turn, built into a microcomputer for program debugging, said trace circuit tracing data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator, said trace circuit comprising:

two trace buffer memories in which the data on the bus of the microcomputer is stored according to the bus clock signal; and

a control circuit storing the data on the bus in said trace buffer memories cyclically and alternately, outputting the data stored from said trace buffer memories cyclically and alternately, wherein the storage of data in and output of data from said trace buffer memories is synchronized with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to the emulator.

7. The trace circuit according to claim 6, wherein said control circuit checks the number of bits of the data on the bus, and, if the number of bits of the data on the bus is no larger than a predetermined value, said control circuit stores the data on the bus in only some of said trace buffer memories, and outputs the data stored in said trace buffer memories, cyclically and in predetermined order.

8. The trace circuit according to claim 7, wherein the predetermined value is 4 bits.

9. The trace circuit according to claim 6 further comprising a bit width conversion circuit connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on bit width of the emulator.

10. The trace circuit according to claim 6 further comprising two output latch circuits respectively connected between said two trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch outputs of said trace buffer memories.